SHRI RAMSWAROOP MEMORIAL UNIVERSITY

End Semester Examination (2021-22)-Odd Semester

M. Tech (CSE) – I Year (I Sem)	
Course Name: Architecture of High Performance Computers	**Code: MEC1010/ MEC1003P**
Time: 02 Hours	**Max Marks: 60**

University Roll No.															

(To be filled by the Student)

Note: Please read instructions carefully:

a) The question paper has 03 sections and it is compulsory to attempt all sections.

b) All questions of Section A are compulsory; questions in Section B and C contain choice.

Section A: Very Short Answer type Questions **Attempt all the questions.**		**BL**	**CLO**	**Marks (10)**
1.	What is meant by addressing mode of an instruction?	BL1	CLO1	02
2.	Demonstrate the following operations- a) 11010-11101 b) 111-110111	BL2	CLO1	02
3.	Illustrate basic Von Neuman Computer Architecture with the help of a diagram.	BL2	CLO3	02
4.	Compare which among the hardwired and micro programmed control unit is faster and why?	BL2	CLO2	02
5.	Explain the role of any two of the following- a)Set Associative Memory b)Cache Memory c)Assembler d)Message Switching Network	BL2	CLO3	02
Section B: Short Answer Type Questions **Attempt any 03 out of 06 questions.**		**BL**	**CLO**	**Marks (30)**
1.	Make use of the tasks T1, T2, T3, T4, T5, T6, T7, T8 to be processed through five segment instruction pipeline. Draw a schematic diagram to illustrate the working of the pipeline and find the total execution time.	BL3	CLO2	10
2.	Illustrate Flynn's Classification for categorizing high performance computers. Which category is not practically possible and why?	BL3	CLO4	10
3.	Examine a machine with 64 MB physical memory and a 32 bit virtual address space. If the page size is 8 KB, Judge the approximate size of	BL4	CLO3	10

	the page table?			
4.	Illustrate an Interrupt? Give examples of instances where interrupts are maskable, How is different from a 'Trap'?	BL4	CLO1	10
5.	Examine the type of Instruction Set possessed by RISC and CISC systems.	BL4	CLO3	10
6.	An array is defined as A[5]={'a','b','c','d','e','f'}. If the address of the second element in A is FF12, compute the address of the fifth element. Assume that the index starts at 0 and character takes one byte of storage. In which register will the final result be stored?	BL3	CLO2	10
Section C: Long Answer Type Questions/Case Study **Attempt any 01 out of 03 questions.**		**BL**	**CLO**	**Marks (20)**
1.	Imagine virtual memory system has page references - 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 0, 1, 1, 7 with 5 page frames. Find number of page faults when following page replacement policies are used– a) LIFO b) FIFO c) LRU	BL6	CLO4	20
2.	Summarize major pipeline hazards and their solutions. Compare the working of a pipelined system with a non-pipelined system.	BL5	CLO3	20
3.	Suppose a set of processors perform following read and write operations on shared variable x and y. Are these operations consistent under some memory consistency model? Justify your answer. P_1: W(x) 3 P_2: W(x) 1 P_3: R(x) 1 R(x) 3 R(y) 0 P_4: W(y) 2	BL6	CLO2	20
